

of the output signal 231 is NOR as clearly shown in Fig. 2g.” Contrarily, however, it is submitted that Sridhar’s Fig. 2b and Fig 2g do not disclose or suggest every element claimed in independent Claim 1. For example, the transmission gate shown in Fig. 2b does not perform an OR operation at the output node 231. This is confirmed by the description on Col. 10, lines 56-57, “Karnaugh map 201 represents the state of node 231.” It can be clearly seen that this Karnaugh map (Fig. 2a of Sridhar et al.) does not reflect an output of an OR operation. Further, it is noted that according to a well known Boolean algebra identity expression, DeMorgan’s Theorem,  $\sim(A+B)$  is equivalent to  $\sim A \cdot \sim B$ . Sridhar et al. appears to be using this theorem in producing its output at 233 of Fig. 2b. That is, Sridhar et al. appears to invert  $A \cdot B$  with its inverter at 232. Accordingly, it appears that the signal that is input to the inverter at 232 is  $A \cdot B$ , not an output of an OR operation. This is explained in Sridhar et al. in Col. 10, lines 45-60 and Col. 11, lines 13-41. Thus, removing the inverter at 232 in Sridhar et al.’s Fig. 2b would not make it function as an OR logic circuit.

For at least the foregoing reasons, it is submitted that Sridhar et al.’s Figs. 2b and 2g do not disclose or suggest a “MOSFET logic circuit for performing a logic OR operation comprising three transistors, first and second transistors of the three transistors forming a transmission gate outputting one signal, and wherein at least two input signals are provided to the first and second transistors and an output signal indicative of an OR operation performed on a first and second input signal of the at least two input signals is output from the MOSFET logic circuit” as claimed in independent Claim 1. Claims 2, 4-9 depend from Claim 1, and therefore, by virtue of their dependencies, it is submitted that these claims are also patentable over Sridhar et al. for at least the same foregoing reasons.

Applicants believe that Claims 1-2, 4-9, are in condition for allowance. If the Examiner has any questions regarding this communication or feels that an interview would be helpful in advancing the prosecution of this application, the Examiner is requested to contact Applicants' undersigned attorney.

Respectfully submitted,



Paul J. Farrell  
Reg. No. 33,494  
Attorney for Applicant

**SEND CORRESPONDENCE TO:**  
DILWORTH & BARRESE, LLP  
333 Earle Ovington Boulevard  
Uniondale, New York 11553  
516-228-8484